Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of the claims in the application:

1. Cancelled

2. (currently amended) ~~The system recited in claim 1~~ A system for validating error detection logic, the system comprising:

a plurality of information paths, each one of the paths having associated therewith an error detection logic, each one of the paths having a plurality of information bits;

a test word buffer for receiving a test word, the test word indicating a particular one of the plurality of information bits in a particular one of the information paths to be corrupted;

a plurality of fault injectors responsive to the test word received by the buffer, each one of the fault injectors being disposed in a corresponding one of the information paths prior to the associated the error detection logic, each one of the fault injectors corrupting a selected one of the information bits in the corresponding one of the information paths in response to the test word received by the buffer to test whether the associated error detection logic detects the injected fault; and

wherein the test word buffer stores an indication as to whether software or a processor used to control information flow through the logic is to be tested for response to a detected fault.

3. (currently amended) A method for testing error detection logic in a system, ~~such~~ the system having a plurality of directors each ~~adapted to handle~~ for handing a data transfer through logic in ~~such~~ the system in accordance with software in ~~such~~ the director, ~~such~~ the software ~~being adapted to deviate~~ for deviating from a normal mode of operation in response to a report of a detected fault by ~~such~~ the error detection logic, ~~such~~ the method comprising:

establishing in the logic a condition for injecting a ~~faults~~ fault into the logic and indicating to ~~such~~ the logic whether the fault is expected ~~anticipated~~ by a designated the one of the directors handling the transfer or ~~unanticipated~~ unexpected by ~~such~~ the designated one of the data transfer handling director;

detecting when the designated one of the directors is handling a data transfer and in response to ~~such~~ the detection injecting a fault into the logic, ~~such~~ the injected ~~faulklt~~ fault being ~~unanticipated~~ expected by the designated director; and

observing whether software in the designated one of the directors responds properly to the injected fault.

4. Canceled

5. (currently amended) A method for validating error detection logic in a system, ~~such~~ the method comprising:

testing whether hardware fault detection logic in the system are responding properly to hardware injected faults;

testing whether software in a designated one of a plurality of directors in ~~such~~the system responds properly to faults injected into the system with ~~such~~ the designated director being ~~*a priori*~~ unaware of the injection of ~~such~~ the fault.

6. Canceled

7. (currently amended) A data storage system wherein data is transferred between a host computer and a bank of disk drives through an interface, ~~such~~ the interface having a plurality of front end directors coupled to the host computer and a plurality of back end directors coupled to the bank of disk drives, ~~such~~ the data passing through a cache memory as ~~such~~ the transferred data passes between the front end directors and the back end directors, ~~such~~the cache memory having control logic coupled between a memory region of the cache memory and the directors, ~~such~~ the system having one of the directors ~~adapted to send~~ for sending test words to the control logic, ~~such~~ the control logic comprising:

(A) a plurality of information paths, each one of ~~such~~ the paths having associated therewith an error detection logic, each one of the paths having a plurality of information bits;

(B) a test word buffer for receiving the test words, ~~such~~ he test words indicating:

(i) a particular one of the plurality of information bits in a particular one of the information paths to be corrupted; and

(ii) whether a hardware test is to be performed on the error detection logic of the control logic or whether a software test is to be performed on the software in a designated one of the directors;

(C) a plurality of fault injectors responsive to the test word received by the buffer, each one of the fault injectors being disposed in a corresponding one of the information paths prior to the associated one of the error detection logics, each one of ~~such~~ the fault injectors corrupting a selected one of the information bits in the corresponding one of the information paths in response to the test word received by the buffer to test whether the associated error detection logic detects ~~such~~ the injected fault, ~~such~~ the associated error detection logic reporting detection of faults to the one of the directors sending the test words when either the hardware test is to be performed or whether the software test on the designated one of the directors.

8. (currently amended) A data storage system wherein data is transferred between a host computer and a bank of disk drives through an interface, ~~such~~ the interface having a plurality of front end directors coupled to the host computer and a plurality of back end directors coupled to the bank of disk drives, ~~such~~ the data passing through a cache memory as ~~such~~ the transferred data passes between the front end directors and the back end directors, ~~such~~ the front end and back end directors being coupled to the cache memory, ~~such~~ the data being transferred as a series of transfers, each one of the transfers having associated therewith a tag, ~~such~~ the tag having a plurality of fields, ~~such~~ the fields identifying: the one of the directors to effect the transfer;; a memory location in the cache memory to store the data being transferred as ~~such~~ the data is transferred through the interface; and, a random number unique in time to the transfer; ~~such~~ the memory having control logic for controlling operation of the memory, respectively, ~~such~~ the control logic being coupled between a memory region of the

memory and the directors, ~~such~~ the system having one of the directors ~~adapted to send~~ for sending test words to the control logic, ~~such~~ the control logic comprising:

(A) a plurality of information paths, each one of ~~such~~ the paths having associated therewith an error detection logic, each one of the paths having a plurality of information bits;

(B) a test word buffer for receiving the test words, ~~such~~ the test words indicating:

(i) a particular one of the plurality of information bits in a particular one of the information paths to be corrupted;

(ii) whether a hardware test is to be performed on the control logic error detection logic or whether a software test is to be performed on the software in a handling one of the directors; and

(iii) wherein ~~such~~ the test word has: a tag data portion and a tag mask portion, ~~such~~ the tag mask portion ~~being adapted to mask~~ for masking a selected one or ones of bits in the fields in a tag of a handling one of the directors;

(C) a plurality of fault injectors responsive to the test word received by the buffer, each one of the fault injectors being disposed in a corresponding one of the information paths prior to the associated the error detection logic, each one of ~~such~~ the fault injectors corrupting a selected one of the information bits in the corresponding one of the information paths in response to the test word received by the buffer to test whether the associated error detection logic detects ~~such~~ the injected fault, ~~such~~the associated error detection logic reporting detection of faults to the one of the directors sending the test words when either the hardware test is to be performed or whether the software test is to be performed on the handling director when ~~such~~ the handling director issuing a tag which when masked by the tag mask portion provides a tag masked portion indicated by the data tag received by the test buffer.

9. (currently amended) The system recited in claim 8 wherein the test word includes an indication of when the fault is to be injected into the fault injector after the initiation of a transfer and the time duration of ~~such~~ the injected fault.

10 (currently amended) The system recited in claim 7 wherein the test word includes an indication of when the fault is to be injected into the fault injector after the initiation of a transfer and the time duration of ~~such~~ the injected fault.